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A HIGH DOPANT CONCENTRATION DIFFUSED RESISTOR AND METHOD OF MANUFACTURE THEREFOR

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CROSS-REFERENCE TO PROVISIONAL APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/326,050 entitled "RESISTOR LOCATED ON A SEMICONDUCTOR SUBSTRATE AND A METHOD OF MANUFACTURE THEREFOR," to Kadaba R. Lakshmikumar, filed on September 28, 2001, which is commonly assigned with the present invention and incorporated herein by reference as if reproduced herein in its entirety.

TECHNICAL FIELD OF THE INVENTION

[0002] The present invention is directed, in general, to integrated circuits and, more specifically, to a high dopant concentration diffused resistor, a method of manufacture therefor, and an integrated circuit including the same.

BACKGROUND OF THE INVENTION

[0003] Over the last several decades, the electronics industry has undergone a revolution by the use of semiconductor technology

to fabricate small, highly integrated electronic devices. Accordingly, a large variety of semiconductor devices having various applicability and numerous disciplines have been manufactured. One such silicon-based semiconductor device that has gained wide use, is the complementary metal oxide semiconductor (CMOS).

[0004] Frequently, CMOS devices are complemented by other devices, such as resistors. For instance, resistors are regularly required in analog CMOS and bipolar CMOS (BiCMOS) semiconductor devices to reduce current spikes associated with such devices. Presently, three broad categories of resistors exist: interconnect resistors, polysilicon resistors, and diffused resistors. Of importance when designing the resistors is precision, resistance values obtainable, low to no voltage dependence and decreased parasitic capacitance. Of the three broad categories of precision resistors, however, only the diffused resistors are consistently capable of providing the precision and resistance values required in today's integrated circuits. For this reason, interconnect resistors and polysilicon resistors are sparingly used.

[0005] Diffused resistors are also commonly broken into three categories: n-well diffused resistors, n+ diffused resistors and p+ diffused resistors, wherein the n+ diffused resistors and p+ diffused resistors are often collectively called high dopant concentration diffused resistors. Of the diffused resistors, the

n-well diffused resistor is the most problematic. Many of the problems associated with the n-well diffused resistors may be ascribed to these resistors being highly voltage dependent. For this reason, n-well diffused resistors are the least desirable of the diffused resistors.

[0006] Turning to Prior Art FIGURE 1, illustrated is a conventional p+ diffused resistor 100 as is currently used in the art. As is shown, the conventional p+ diffused resistor 100 includes a conventional n-well 120 formed within a semiconductor substrate 110. As is further illustrated, a p+ resistor region 130 is formed within the n-well 120, wherein the p+ resistor region 130 has contacts 140 contacting either side thereof.

[0007] Turning to Prior Art FIGURE 2, illustrated is a conventional n+ diffused resistor 200 as is currently used in the art. The n+ diffused resistor 200, in comparison to the p+ diffused resistor 100, does not include the n-well 120 (FIGURE 1), but its n+ resistor region 220 is formed directly in its semiconductor substrate 210. Because the semiconductor substrate 210 is p-type doped, the n+ resistor region 220 is sufficiently isolated without using the n-well 120 (FIGURE 1).

[0008] While both the p+ and n+ diffused resistors 100, 200, are much more desirable than the standard n-well diffused resistor (and especially the interconnect resistors and polysilicon resistors), they do have certain drawbacks. For example, it has been observed

that the p+ and n+ diffused resistors 100, 200, do not function as accurately and precisely as required for many of the high frequency devices being manufactured today. More specifically, it has been observed that the bandwidth of the high frequency devices is limited by certain features of the diffused resistors, mainly capacitances that form at the junction between the n-well 120 and the p+ resistor region 130, and the semiconductor substrate 210 and n+ resistor region 220, for the p+ diffused resistor 100 and n+ diffused resistor 200, respectively.

[0009] Accordingly, what is needed in the art is a p+ or n+ diffused resistor that may be used in conjunction with higher frequency devices, and that does not experience the parasitic capacitance problems addressed above.

SUMMARY OF THE INVENTION

[0010] To address the above-discussed deficiencies of the prior art, the present invention provides a high dopant concentration diffused resistor, a method of manufacture therefor, and an integrated circuit including the same. In one embodiment of the invention, the high dopant concentration diffused resistor includes a doped tub located over a semiconductor substrate and a doped resistor region located in the doped tub, the doped resistor region forming a junction within the doped tub. In a related embodiment, the high dopant concentration diffused resistor further includes first and second terminals each contacting the doped tub and the doped resistor region, wherein the first and second terminals cause the doped tub and doped resistor region to have a zero potential difference at any point across the junction when a voltage is applied to the first and second terminals. Often, this may be accomplished without adding additional processing steps.

[0011] In an alternative embodiment of the invention, the high dopant concentration diffused resistor includes a doped tub located over a semiconductor substrate and having a concentration of a first dopant, and a doped resistor region located in the doped tub and having a higher concentration of the first dopant. In a similar embodiment, the resistor further includes a first terminal contacting the doped resistor region at a first location and an

opposing second terminal contacting the doped resistor region at a second location, wherein the similar dopant between the doped tub and doped resistor region cause them to have a zero potential difference at any point across a junction therebetween when a voltage is applied to the first and second terminals.

[0012] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The invention is best understood from the following detailed description when read with the accompanying FIGUREs. It is emphasized that in accordance with the standard practice in the semiconductor industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0014] FIGURE 1 illustrates a Prior Art p+ diffused resistor;

[0015] FIGURE 2 illustrates a Prior Art n+ diffused resistor;

[0016] FIGURE 3 illustrates a partially completed integrated circuit constructed in accordance with the principles of the present invention, including a high dopant concentration diffused resistor located on a semiconductor substrate;

[0017] FIGURE 4 illustrates a partially completed high dopant concentration diffused resistor constructed in accordance with the principles of the present invention, and more specifically, the formation of a doped resistor region;

[0018] FIGURE 5 illustrates the partially completed high dopant concentration diffused resistor illustrated in FIGURE 4, after formation of a first terminal and a second terminal, each contacting both the doped resistor region and a doped tub;

[0019] FIGURE 6 illustrates a diagram showing the parallel resistors formed as a result of the first and second terminal formation of FIGURE 5;

[0020] FIGURE 7 illustrates a partially completed n+ diffused resistor in accordance with the principles of the present invention;

[0021] FIGURE 8 illustrates a diagram showing the parallel resistors formed as a result of the similar dopant type used for the doped tub and the doped resistor region;

[0022] FIGURE 9 illustrates an embodiment of the advantages realized by the p+ or n+ diffused resistors of FIGUREs 3 and 7; and

[0023] FIGURE 10 illustrates a completed integrated circuit, which provides one environment where the resistor may be included.

DETAILED DESCRIPTION

[0024] Referring initially to FIGURE 3, illustrated is a cross-sectional view of a partially completed integrated circuit 300 constructed in accordance with the principles of the present invention. The partially completed integrated circuit 300 in the embodiment illustrated in FIGURE 3 includes a completed high dopant concentration diffused resistor located over a semiconductor substrate 315, wherein the high dopant concentration diffused resistor in this embodiment happens to be a p+ diffused resistor 310. While the present embodiment focuses on the p+ diffused resistor 310, those skilled in the art understand that any known or hereafter discovered high dopant concentration diffused resistor could be used. In an advantageous embodiment, the completed p+ diffused resistor 310 includes a doped tub 320 located over the semiconductor substrate 315, and a doped resistor region 325 located within the doped tub 320. The completed p+ diffused resistor 310, as illustrated, further includes a first terminal 330 that contacts the doped tub 320 and the doped resistor region 325, and an opposing second terminal 335 that contacts the doped tub 320 and the doped resistor region 325.

[0025] Included within the doped tub 320 and the doped resistor region 325 are a first dopant, and a second dopant opposite to the first dopant, respectively. In the particular embodiment shown in

FIGURE 3, the first dopant comprises an n-type dopant and the second dopant comprises a p-type dopant. Similarly, the semiconductor substrate 315 may comprise the p-type dopant.

[0026] In the illustrative embodiment of FIGURE 3, ohmic contacts 332, 337, are located at points where the first and second terminals 330, 335, contact the doped tub 320. As those skilled in the art understand, the ohmic contacts 332, 337, may be island regions having a higher dopant concentration of the first dopant than the doped tub 320. Other ohmic contacts 332, 327, are, however, within the scope of the present invention. Also included within the partially completed integrated circuit 300 illustrated in FIGURE 3 are conventionally formed transistor regions 350, 360.

[0027] It has presently been found that the conventional p+ and n+ diffused resistors 100, 200, illustrated in FIGUREs 1 and 2 have parasitic capacitances associated therewith. It is believed that the parasitic capacitance arises because of a depletion region that forms at a p-n junction of each. The depletion region, in such an instance, tends to behave like an insulator located between two conductors, wherein the doped resistor region and the tub region behave like the two conductors. It is thought that a voltage differential across the p-n junction associated with diffused resistor tends to cause undesirable current leakage and power dissipation in high frequency semiconductor devices.

[0028] Accordingly, it has been found that by negating or counterbalancing the voltage differential associated with such high frequency semiconductor devices, the parasitic capacitance is substantially reduced. The exemplary resistor of FIGURE 3, which is within the scope of the present invention, substantially diminishes the voltage differential across the doped tub 320 and doped resistor region 325, by using the first terminal 330 that contacts the doped tub 320 and the doped resistor region 325, and the opposing second terminal 335 that contacts the doped tub 320 and the doped resistor region 325. This unique configuration substantially negates or counterbalances the effective parasitic capacitance. For example, at any line 340 drawn perpendicularly through the p-n junction of the doped tub 320 and the doped resistor region 325, a substantially similar voltage may be realized. Accordingly, the first and second terminals 330, 335 cause the doped tub 320 and doped resistor region 325 to have a zero potential difference at any point across a junction therebetween, when a voltage is applied to the first and second terminals 330, 335.

[0029] Turning to FIGUREs 4 and 5, illustrated are detailed manufacturing steps illustrating how one skilled in the art might manufacture a device similar to the partially completed integrated circuit illustrated in FIGURE 3. FIGURE 4 illustrates a cross-sectional view of a partially completed integrated circuit 400 at

an intermediate manufacturing step. The partially completed integrated circuit 400 includes a partially completed p+ diffused resistor region 410, and conventional transistor regions 450, 480, all of which are located over a semiconductor substrate 415. By way of example, the transistor regions 450, 480 may be located adjacent the partially completed p+ diffused resistor region 410. However, other design layouts are also within the scope of the present invention.

[0030] The semiconductor substrate 415 may, in an exemplary embodiment, be any layer located in the integrated circuit 400, including a wafer itself or a layer located above the wafer. In the embodiment illustrated in FIGURE 4, the semiconductor substrate 415 is a p-type substrate; however, one skilled in the art understands that the semiconductor substrate 415 could be an n-type substrate, without departing from the scope of the present invention. It should also be noted that in an exemplary embodiment the semiconductor substrate 415 may be grounded.

[0031] In the embodiment shown in FIGURE 4, the transistor regions 450, 480, include an n-type transistor tub 455 and a p-type transistor tub 485, respectively. The type of dopant used to form the transistor tubs may, however, be reversed without departing from the scope of the present invention. One having skill in the art understands how to form the n-type transistor tub 455 and the p-type transistor tub 485, including protecting a region with a

photoresist mask and subjecting an unprotected region to a desired dopant.

[0032] The transistor regions 450, 480, further include conventionally formed source and drain regions 460, 490, respectively. In the embodiment that includes the n-type transistor tub 455 and the p-type transistor tub 485, the source and drain regions 460, 490 would be p-type doped and n-type doped, respectively. It should be well understood, however, in the case where the dopant included within the transistor tubs is reversed, the dopant included within the source and drain regions 460, 490, would also be reversed. The transistor regions 450, 480, may further include conventional transistors 495, including gate oxides, polysilicon gates and oxide spacers.

[0033] As previously stated, the partially completed integrated circuit 400 includes the partially completed p+ diffused resistor region 410. The partially completed p+ diffused resistor region 410 includes a doped tub 420. The doped tub 420, in a previous step not shown, was doped with a first dopant. In an exemplary embodiment of the invention, the first dopant is an n-type dopant, for example phosphorous or arsenic, and is doped to a concentration of about 1E16 atoms/cm^3 to about 1E17 atoms/cm^3. It should be noted, however, in situations where the semiconductor substrate 415 is an n-type semiconductor substrate, as discussed above, the first dopant would comprise a p-type dopant having a concentration of

about 1E16 atoms/cm^3 to about 1E17 atoms/cm^3. One having skill in the art understands the desire to have opposite dopant types for the doped tub 420 and the semiconductor substrate 415. Advantageously, the doped tub 420 may be formed concurrently with the similarly doped n-type transistor tub region 455. One having skill in the art understands how this may be accomplished with various masking steps. This aspect of the present invention is, of course, desirable because the concurrent formation of the doped tub 420 and the similarly doped n-type transistor tub region 455 saves valuable time and money.

[0034] Also included within the partially completed p+ diffused resistor region 410 is a doped resistor region 425 located within the doped tub 420. The doped resistor region 425, in an exemplary embodiment, includes a second dopant, opposite to that of the first dopant included within the doped tub 420. Thus, in situations where the doped tub 420 includes the n-type dopant, the doped resistor region 425 would include a p-type dopant, such as boron. The inverse would, again, also hold true where the doped tub 420 includes the p-type dopant and the semiconductor substrate 415 is an n-type substrate. The second dopant may have a concentration ranging from about 1E18 atoms/cm^3 to about 1E19 atoms/cm^3, which is similar to the dopant concentration included within the source and drain regions 460, 490. In the illustrative embodiment shown in FIGURE 4, the doped resistor region 425 may be formed concurrently

with the similarly doped source and drain regions 460. While it is desirable that the doped resistor region 425 and the similarly doped source and drain regions 460 be concurrently formed, it should be noted that the doped resistor region 425 may nonetheless be formed in an independent manufacturing step.

[0035] Turning now to FIGURE 5, illustrated is a cross-sectional view of the partially completed integrated circuit 400 illustrated in FIGURE 4, after formation of a first terminal 510 and an opposing second terminal 520. The first terminal 510 and the opposing second terminal 520 are formed in a conventionally deposited interlevel dielectric layer 530 that overlays both the conventional transistors 495 and the partially completed p+ diffused resistor region 410. The first terminal 510 and the opposing second terminal 520 may be formed using conventional photolithographic processes to develop vias in the interlevel dielectric. Once the vias are formed, they are then filled with a conductive material, such as metal, and patterned with conventional processes to complete the terminals 510 and 520.

[0036] One skilled in the art understands the processes by which the layer of interconnect material may be formed, including conventional chemical vapor deposition (CVD), physical vapor deposition (PVD), or other similar known processes. The layer of interconnect material may comprise any known or hereinafter

discovered conductive material generally used in the manufacture of semiconductor devices.

[0037] As illustrated in FIGURE 5, the first terminal 510 contacts the doped tub 420 and the doped resistor region 425, while the opposing second terminal 520 also contacts the doped tub 420 and the doped resistor region 425. Turning briefly to FIGURE 6, with continued reference to FIGURE 5, illustrated is a circuit diagram 600 representing the p+ resistor region 410 illustrated in FIGURE 5. As a result of the unique terminal configuration, the doped tub 420 behaves like a tub resistor 610, wired in parallel with the doped resistor region 425. As illustrated, there is no voltage differential across the tub resistor 610 and the doped resistor region 425. In accordance with the principles of the present invention, this substantially reduces the parasitic capacitance, and therefore, substantially reduces the current leakage and power dissipation associated with the p+ resistor region 410. Even though it is shown that there is a distributed capacitance 620 between the doped tub 420 (e.g., the tub resistor 610) and the semiconductor substrate 415, the capacitance is relatively small because of the reduced dopant concentrations of the two layers.

[0038] Turning now to FIGURE 7, illustrated is a cross-sectional view of an alternative embodiment of a partially completed integrated circuit 700 constructed in accordance with the

principles of the present invention. The partially completed integrated circuit 700 in the embodiment illustrated in FIGURE 7 includes an alternative embodiment of the completed high dopant concentration diffused resistor illustrated in FIGURE 3. The partially completed integrated circuit 700 in the embodiment illustrated in FIGURE 7 includes a completed n+ diffused resistor region 710 located over a semiconductor substrate 715. In an advantageous embodiment, the completed n+ diffused resistor region 710 includes a doped tub 720 located over the semiconductor substrate 715, and a doped resistor region 725 located within the doped tub 720.

[0039] In the particular embodiment shown, the doped tub 720 and the doped resistor region 725 both include the same type of dopant, however, the doped resistor region 725 includes a higher concentration of the dopant than the doped tub 720. For instance, in an exemplary embodiment the doped tub 720 includes an n-type dopant having a concentration of about 1E16 atoms/cm^3 to about 1E17 atoms/cm^3, while the doped resistor region 725 includes the n-type dopant to a concentration ranging from about 1E18 atoms/cm^3 to about 1E19 atoms/cm^3.

[0040] The completed n+ diffused resistor region 710, as illustrated, further includes a first terminal 730 that contacts the doped resistor region 725, and an opposing second terminal 735 that also contacts the doped resistor region 725. In contrast to

the embodiment shown in FIGURE 3, the first and second terminals 730, 735, do not also actually physically contact the doped tub 720. Nonetheless, the similar dopant between the doped tub 720 and the doped resistor region 725 causes them to have a substantially equal potential value at any two adjacent points on either side of the doped tub 720 / doped resistor region 725 junction. Saying it another way, the similar dopant between the doped tub 720 and doped resistor region 725 causes them to have a zero potential difference at any point across a junction therebetween, when a voltage is applied to the first and second terminals 730, 735. Accordingly, the parasitic capacitance of the n+ diffused resistor region 710 is substantially reduced, similar to the p+ diffused resistor 310 of FIGURE 3.

[0041] Turning briefly to FIGURE 8, with continued reference to FIGURE 7, illustrated is a circuit diagram 800 representing the n+ diffused resistor region 710 illustrated in FIGURE 7. As a result of the similar dopant type between the doped tub 720 and the doped resistor region 725, and therefore conductivity therebetween, the doped tub 720 behaves like a tub resistor 810, wired in parallel with the doped resistor region 725. As illustrated, there is no voltage differential across the doped tub 720 and the doped resistor region 725, which substantially reduces the parasitic capacitance, and therefore, substantially reduces the current leakage and power dissipation associated with the n+ diffused

resistor region 710. Even though it is shown that there is a distributed capacitance 820 between the doped tub 720 (e.g., the tub resistor 810) and the semiconductor substrate 715, the capacitance is relatively small because of the reduced dopant concentrations of the two layers. Further, current flowing through the doped tub 720 is also small because of its higher resistance. Accordingly, the net effect is quite beneficial.

[0042] Turning now to FIGURE 9, illustrated is a graph 900 illustrating one example of the benefits that may be realized using various aspects of the present invention. Graph 900 compares the frequency response of a novel n+ diffused resistor similar to that of FIGURE 7 (e.g., with a doped tub underneath), to that of a conventional n+ diffused resistor (e.g., without a doped tub underneath). In the illustrative embodiment, line 910 represents the novel device and line 920 represents the conventional device. Graph 900 clearly shows that the bandwidth attainable at -3dB for the conventional device is half of what is attainable for the novel device. As is noticed, similar benefits may be achieved at other voltages.

[0043] Turning briefly to FIGURE 10, with reference to FIGURE 3, there is illustrated a cross-sectional view of a conventional integrated circuit 1000 that might include a completed resistor, similar to the above described completed resistor 310. The integrated circuit 1000 may include a CMOS device, a BiCMOS device,

or other type of integrated circuit device. Shown in FIGURE 10 are components of the conventional integrated circuit 1000, including: the transistor regions 350, 360, and dielectric layers 1010, in which interconnect structures 1020 are formed (together forming interconnect layers). Also included in the integrated circuit 1000 is the previously mentioned completed resistor 310, formed upon the semiconductor substrate 315. In the embodiment shown in FIGURE 10, the interconnect structures 1020 connect the transistor regions 350, 360, to other areas of the integrated circuit 1000. Also shown in the integrated circuit 1000 illustrated in FIGURE 10, are conventionally formed transistor tubs 1030, 1040, and source/drain regions 1050, 1060, respectively.

[0044] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.